AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

1. (currently amended) A semiconductor data processing device for connecting a non-volatile storage device to a general-purpose bus of a host system, in which said data processing device enters an active state or standby state in response to a state of said general-purpose bus,

said data processing device comprising:

a clock circuit for stopping an internal clock signal in said standby state; ~~and~~

a voltage generation circuit for applying a substrate bias voltage in a direction for reducing a threshold leak current in said standby state;

a rewritable non-volatile memory for storing a control program that connecting said non-volatile storage device to said general-purpose bus;

a rewritable non-volatile memory for storing a control program that connecting said non-volatile storage device to said general-purpose bus;

a central processing unit for executing said control program,

wherein said central processing unit and said non-volatile memory receive said substrate bias voltage;

a circuit for detecting the state of said general-purpose bus to control state changes from said standby state to said active state;

wherein said substrate bias voltage is not applied to any of this circuit and said voltage generation circuit

a first interface controller that interfaces with said non-volatile storage device;

a second interface controller that interfaces with said general-purpose bus; and

a data transfer controller for controlling data transfer between said first interface controller and said second interface controller;

wherein said first and second interface controllers, as well as said data transfer controller input/output parallel data in units of 2n bits while said central processing unit inputs/outputs parallel data in units of n bits or below.

2-8. (cancelled)

9. (currently amended) The semiconductor data processing device according to claim ~~8~~1,

wherein said data transfer controller is connected to a 2n-bit first data bus while said central processing unit is connected to either the lower part or upper part of said first data bus.

10. (original) The semiconductor data processing device according to claim 9,

wherein said first and second interface controllers are connected to a 2n-bit second data bus respectively,

wherein said processing device further includes a first data bus for connecting said first data bus to said second data bus, and

wherein said bus controller fixes the correspondence between each signal line of said second bus and the bit position of access data and varies the correspondence between each signal line of said first data bus and the bit position of access data according to each access data size.

11. (currently amended) A semiconductor data processing device, comprising:

a central processing unit; ~~and~~

a rewritable non-volatile memory for storing a program to be executed by said central processing unit,

wherein an internal clock signal is stopped and a substrate bias voltage is applied in a direction for increasing a threshold voltage in the standby state, and said substrate bias voltage is also applied to said central processing unit and said non-volatile memory;

first and second interface controllers controlled by said central processing unit; and

a data transfer controller capable of controlling data transfer between said first and second interface controllers;

wherein said first and second interface controllers, as well as said data transfer controller input/output parallel data in units of 2n bits while said central processing unit inputs/outputs parallel data in units of n bits or below.

12. (cancelled)

13. (currently amended) The semiconductor data processing device according to claim ~~12~~11,

wherein said first interface controller is a memory card interface controller.

14. (currently amended) The semiconductor data processing device according to claim ~~12~~11,

wherein said second interface controller is a USB interface controller.

15. (cancelled)

16. (currently amended) The semiconductor data processing device according to claim ~~15~~11,

wherein said data transfer controller is connected to a 2n-bit first data bus while the central processing unit is connected to either the lower or upper part of said first data bus.

17. (original) The semiconductor data processing device according to claim 16,

wherein said first and second interface controllers are connected to a 2n-bit second data bus respectively,

wherein said processing device includes a bus controller for connecting said first data bus to said second data bus, and

wherein said bus controller fixes the correspondence between each signal line of said second bus and the bit

position of access data and varies the correspondence between each signal line of said first data bus and the bit position of access data according to the access data size.

18-23. (cancelled)

24. (currently amended) A semiconductor data processing device, comprising:

a central processing unit;

a non-volatile memory for storing a control program to be executed in said central processing unit, said memory capable of writing and erasing data therein/therefrom electrically;

a clock generation circuit; ~~and~~

a first control circuit, and

a peripheral circuit,

wherein said clock generation circuit stops generation of said clock when said data processing device enters said standby state while said first control circuit controls said central processing unit, said non-volatile memory, and said clock generation circuit so as to reduce a sub-threshold leak current in each MOS transistor constituting said central processing unit, said non-volatile memory, and said clock generation circuit,

wherein said first control circuit receives first and second supply potentials to be driven to operate regardless of whether said data processing device is in said standby state or not,

wherein said peripheral circuit includes a first detection circuit for detecting the state of a bus to which it is be connected,

wherein said first control circuit controls the elements of said peripheral circuit except for said first detection circuit in response to said standby state, and

wherein said first detection circuit receives first and second supply potentials to be driven to operate regardless of whether or not said data processing device is in said standby state;

wherein said processing device further includes a second control circuit,

wherein said second control circuit includes a second detection circuit for detecting the output of said first detection circuit,

wherein said first control circuit controls circuit elements of said second control circuit other than said second detection circuit in response to said standby state, and

wherein said second detection circuit receives said first and second supply potentials to be driven to operate regardless of whether or not said data processing device is in said standby state.

25-36. (cancelled)

37. (new) A semiconductor data processing device, comprising:

a central processing unit;

a non-volatile memory for storing a control program to be executed in said central processing unit, said memory capable of writing and erasing data therein/therefrom electrically;

a clock generation circuit;

a first control circuit, and

a peripheral circuit,

wherein said clock generation circuit stops generation of said clock when said data processing device enters said standby state while said first control circuit controls said central processing unit, said non-volatile memory, and said clock generation circuit so as to reduce a sub-threshold

leak current in each MOS transistor constituting said central processing unit, said non-volatile memory, and said clock generation circuit,

wherein said first control circuit receives first and second supply potentials to be driven to operate regardless of whether said data processing device is in said standby state or not,

wherein said peripheral circuit includes a first detection circuit for detecting the state of a bus to which it is be connected,

wherein said first control circuit controls the elements of said peripheral circuit except for said first detection circuit in response to said standby state, and

wherein said first detection circuit receives first and second supply potentials to be driven to operate regardless of whether or not said data processing device is in said standby state,

wherein said semiconductor data processing device further includes a second control circuit,

wherein said second control circuit includes a second detection circuit for detecting the state of said first detection circuit,

wherein said first control circuit controls elements of said second control circuit except for said second detection circuit in response to said standby state, and

wherein said second detection circuit receives said first and second supply potentials and is driven to operate regardless of said standby state.

38. (new) A semiconductor data processing device for connecting a non-volatile storage device to a general-purpose bus of a host system, in which said data processing device enters an active state or standby state in response to a state of said general-purpose bus,

said data processing device comprising:

a clock circuit for stopping an internal clock signal in said standby state;

a voltage generation circuit for applying a substrate bias voltage in a direction for reducing a threshold leak current in said standby state;

a rewritable non-volatile memory for storing a control program that connecting said non-volatile storage device to said general-purpose bus;

a rewritable non-volatile memory for storing a control program that connecting said non-volatile storage device to said general-purpose bus;

a central processing unit for executing said control program;

wherein said central processing unit and said non-volatile memory receive said substrate bias voltage;

a circuit for detecting the state of said general-purpose bus to control state changes from said standby state to said active state;

wherein said substrate bias voltage is not applied to any of this circuit and said voltage generation circuit;

a first interface controller that interfaces with said non-volatile storage device;

a second interface controller that interfaces with said general-purpose bus;

wherein said first interface controller is a memory card interface controller and said second interface controller is a USB interface controller; and

a data transfer controller for controlling data transfer between said first interface controller and said second interface controller;

wherein said first and second interface controllers, as well as said data transfer controller input/output parallel

data in units of 2n bits while said central processing unit inputs/outputs parallel data in units of n bits or below.

39. (new) The semiconductor data processing device according to claim 38,

wherein said data transfer controller is connected to a 2n-bit first data bus while said central processing unit is connected to either the lower part or upper part of said first data bus.

40. (new) The semiconductor data processing device according to claim 39,

wherein said first and second interface controllers are connected to a 2n-bit second data bus respectively,

wherein said processing device further includes a first data bus for connecting said first data bus to said second data bus, and

wherein said bus controller fixes the correspondence between each signal line of said second bus and the bit position of access data and varies the correspondence between each signal line of said first data bus and the bit position of access data according to each access data size.